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Japanese Patent Laid-Open Publication No. Heisei 9-8205

(TITLE OF THE INVENTION)

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

5

(CLAIMS)

1. A resin-encapsulated semiconductor device using
a lead frame which is shaped in accordance with a two-step
etching process to a body wherein a thickness of inner
10 leads is less than that of the lead frame blank,
comprising:

inner leads having the thickness less than that of the
lead frame blank; and

15 terminal columns integrally connected to the inner
leads and having the same thickness with the lead frame
blank, the terminal columns possessing a column-shaped
configuration which is adapted to be electrically connected
to an external circuit, the terminal columns being disposed
20 outside of the inner leads in a manner such that they are
coupled to the inner leads in a direction orthogonal to the
thickness-wise direction thereof, the terminal columns
having terminal portions arranged on top ends thereof, the
terminal portions being made of solders, etc. and exposed
25 to the outside beyond a resin encapsulate, each inner lead
possessing a rectangular cross-section and having four

surfaces including a first surface, a second surface, a
third surface and a fourth surface, the first surface being
flushed with one surface of a remaining portion of the
inner lead having the same thickness with the lead frame
blank while being opposed to the second surface, and each
5 of the third and fourth surfaces having a concave shape
depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using
10 a lead frame which is shaped in accordance with a two-step
etching process to a body wherein a thickness of inner
leads is less than that of the lead frame blank,
comprising:

inner leads having the thickness less than that of the
15 lead frame blank; and

terminal columns integrally connected to the inner
leads and having the same thickness with the lead frame
blank, the terminal columns possessing a column-shaped
configuration which is adapted to be electrically connected
20 to an external circuit, the terminal columns being disposed
outside of the inner leads in a manner such that they are
coupled to the inner leads in a direction orthogonal to the
thickness-wise direction thereof, portions of top ends of
the terminal columns being exposed to the outside beyond a
25 resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank, while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

3. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

4. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

5. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

6. The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively.

7. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein the semiconductor chip is fastened to the second surfaces of the inner leads by bumps, thereby to be electrically connected to the inner leads.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[DESCRIPTION OF THE PRIOR ART]

FIG. 15(a) shows the configuration of a generally known resin-encapsulated semiconductor device (a plastic lead frame package). The shown resin-encapsulated semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1511
to be electrically connected to the associated circuits,
inner leads 1512 formed integrally with the outer leads
1511, bonding wires 1530 for electrically connecting the
tips of the inner leads 1512 to the bonding pad 1521 of the
semiconductor chip 1520, and a resin 1540 encapsulating the
semiconductor chip 1520 to protect the semiconductor chip
1520 from external stresses and contaminants. This resin-
encapsulated semiconductor device, after mounting the
semiconductor chip 1520 on the bonding pad 1521, is
manufactured by encapsulating the semiconductor chip 1520
with the resin. In this resin-encapsulated semiconductor
device, the number of the inner leads 1512 is equal to that
of the bonding pads 1521 of the semiconductor chip 1520.
And, FIG. 15(b) shows the configuration of a monolayer lead
frame used as an assembly member of the resin-encapsulated
semiconductor device shown in FIG. 15a. Such a lead frame
includes the bonding pad 1511 for mounting the
semiconductor chip, the inner leads 1512 to be electrically
connected to the semiconductor chip, the outer lead 1513
which is integral with the inner leads 1512 and is to be
electrically connected to the associated circuits. This
also includes dam bars 1514 serving as a dam when
encapsulating the semiconductor chip with the resin, and a
frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal
such as a cobalt, 42 alloy (a 42% Ni-Fe alloy), copper-based
alloy by a pressing working process or an etching process.
FIG. 15(b)(D) is a cross-sectional view taken along the
5 line F1-F2 of FIG. 15(b)(1).

Recently, there has been growing demand for the
miniaturization and reduction in thickness of resin-
encapsulated semiconductor device employing lead frames
like the lead frame (plastic lead frame package) and the
10 increase of the number of terminals of resin-encapsulated
semiconductor package as electronic apparatuses are
miniaturized progressively and the degree of the
integration of semiconductor device increase progressively.
Thus, recent resin-encapsulated semiconductor package,
15 particularly quad plate package (QFPs) and thin quad flat
packages (TQFPs) have each a greatly increased number of
pins.

Lead frames having inner leads arranged at small
pitches among lead frames for semiconductor packages are
20 fabricated by a photolithographic etching process, while
lead frames having inner leads arranged at comparatively
large pitches among lead frames for semiconductor packages
are fabricated by press working. However, lead frames
having a large number of fine inner leads to be used for
25 forming semiconductor packages having a large number of

pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, a photoresist, such as a water-soluble casein photoresist containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant containing ferric chloride as a principal component is sprayed against the thin sheet 1410 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1020 so that inner leads of predetermined sizes and shapes are formed as shown in FIG. 14(d).

Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100% of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80 μ m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm is used and inner leads are formed by etching so that the

fine tips thereof are arranged at a pitch of about 0.1 mm.

However, recent miniature resin-encapsulated semiconductor package requires inner leads arranged
5 pitches in the range of 0.13 to 0.15 mm, far smaller than 0.165 mm. When a lead frame is fabricated by processing thin sheet of a reduced thickness, the strength of the outer leads of such a lead frame is not large enough
10 to withstand external forces that may be applied thereto in the subsequent processes including an assembling process and a chip mounting process. Accordingly, there is a limit to the reduction of the thickness of the thin sheet to enable the fabrication of a minute lead frame having fine leads arranged at very small pitches by etching.

15 An etching method previously proposed to overcome such difficulties subjects a thin sheet to an etching process to form a lead frame after reducing the thickness of portions of the thin sheet corresponding to the inner leads of the lead frame by half etching or pressing to form
20 the fine inner leads by etching without reducing the strength of the outer leads. However, problems arise in accuracy in the subsequent processes when the lead frame is formed by etching after reducing the thickness of the portions corresponding to the inner leads by pressing; for
25 example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

(SUBJECT MATTERS TO BE SOLVED BY THE INVENTION)

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting process. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals

and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[MEANS FOR SOLVING THE SUBJECT MATTERS]

5 According to one aspect of the present invention, there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than
10 of the lead frame blank; and terminal columns electrically connected to the inner leads and having the same thickness as with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be
15 electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions
20 arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond the resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead possessing a rectangular
25 cross-section and having four surfaces including a

surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surf-
of a remaining portion of the inner lead having the same
thickness with the lead frame blank while being opposed
the second surface, and each of the third and fourth
surfaces having a concave shape depressed toward the inside
of the inner lead.

According to another aspect of the present invention
there is provided a resin-encapsulated semiconductor device
using a lead frame which is shaped in accordance with
two-step etching process to a body wherein a thickness of
inner leads is less than that of the lead frame blank
comprising: inner leads having the thickness less than that
of the lead frame blank; and terminal columns integrally
connected to the inner leads and having the same thickness
with the lead frame blank, the terminal columns possessing
a column-shaped configuration which is adapted to be
electrically connected to an external circuit, the terminal
columns being disposed outside of the inner leads in a
manner such that they are coupled to the inner leads in a
direction orthogonal to the thickness-wise direction
thereof, portions of top ends of the terminal columns being
exposed to the outside beyond a resin encapsulate, outer
surfaces of the terminal columns also being exposed to the
outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention, a semiconductor chip is received inward of the inner leads, and electrodes (pads) of the semiconductor chip are electrically connected to the inner leads through wires, respectively. According to another aspect of the present invention, the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad. According to another aspect of the present invention, the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape. According to still another aspect of the present invention, the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

20 (WORKING FUNCTIONS)

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the forming process of the outer leads as in the case of using

a mono-layered lead frame shown in FIG. 13(b) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and coplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding process can be enlarged.

(EMBODIMENTS)

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, a resin-encapsulated semiconductor device in accordance

With a first embodiment of the present invention described hereinafter with reference to FIGS. 1 and 2, FIG. 1(a) is a cross-sectional view of the encapsulated semiconductor device according to the embodiment of the present invention. FIG. 1(b) is a sectional view of an inner lead taken along the line of FIG. 1(a), and FIG. 1(c) is a cross-sectional view of a terminal column taken along the line B1-B2 of FIG. 1(a). Moreover, FIG. 2(a) is a perspective view of the encapsulated semiconductor device according to the embodiment of the present invention, FIG. 2(b) is a top view of the resin-encapsulated semiconductor device of FIG. 2(a), and FIG. 2(c) is a bottom view of the encapsulated semiconductor device of FIG. 2(a). In FIGS. 1 and 2, a drawing reference numeral 100 represents an encapsulated semiconductor device, 110 a semiconductor chip, 111 electrodes (pads), 120 wires, 130 a lead, 131 inner leads, 131Aa a first surface, 131Ab a second surface, 131Ac a third surface, 131Ad a fourth surface, 133A terminal columns, 133B terminal portions, 133C top surfaces, 133S a top surface, 135 a die pad, and 140 a resin encapsulate.

In the resin-encapsulated semiconductor device according to the first embodiment, as shown in FIG. 1, the semiconductor chip 110 is placed inward of the

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 133 at one surface thereof which is opposed to the other surface thereof where the electrodes pads 111 of the semiconductor chip 110 are arranged. Each electrode pad 111 is electrically connected to the second surface 131A of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133A located on the top surfaces 133S of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-iron alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 or other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 9A is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40 μ m whereas the portions of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire bonding thereon. Also, as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed.

In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the
inner leads 131 is long or not. The inner leads having the
contour, as shown in FIG. 9(a), in which the tips of the
inner leads 131 are separated one from another, are
5 prepared by the etching process, and the inner leads are
resin-encapsulated after mounting the semiconductor chip
thereon as will be described later. However, where the
inner leads 131 are long in their length and have a
tendency for the generation of twisting therein, it is
10 impossible to fabricate the lead frame by etching to have
the contour as shown in FIG. 9(a). Therefore, after
etching the lead frame in a state where the tips of the
inner leads are fixed to the connecting portion 131B as
shown in FIG. 9(c)(1), the inner leads 131 are fixed with
15 the reinforcing tape 160 as shown in FIG. 9(c)(2). Then,
the connecting portions 131B which are not necessary in the
fabrication of the resin-encapsulated semiconductor device
are removed by a press as shown in FIG. 9(c)(3), and a
semiconductor device is then mounted on the lead frame.

20 Hereinafter, a method for the fabrication of the
resin-encapsulated semiconductor device will now be
described with reference to FIG. 8. First, the lead frame
130A, as shown in FIG. 9(a), which is shaped by the etching
process as will be described later, is prepared such that
25 the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131Ab of the inner leads 131 are bonded with each other using wires 120 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press to form terminal columns 133 and also the side surfaces 133B of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi-spherical solder are arranged on the outer surface of each terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the resultant structure in such a manner that the side surfaces

of the terminal columns 133 are covered thereby (FIG. 6(f)). At this time, the protective frame 180 functions to reinforce the semiconductor device. In other words, the protective frame 180 serves to prevent moisture from leaking into a gap between the resin encapsulate and the terminal columns due to the fact that the side surfaces of the terminal columns are exposed to the outside, whereby a crack is not formed in the semiconductor device and the breakage of the semiconductor device is avoided. However, persons skilled in the art will readily appreciate that it is not necessarily required to provide the protective frame 180. Also, when such an encapsulating process by the resin is carried out using a desired mold, the encapsulating process is implemented in a state wherein the outer side surfaces of the terminal columns of the lead frame are somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first embodiment will now be described in conjunction with the attached drawings. FIG. 11 is of cross-sectional views respectively illustrating sequential steps of the etching process for the lead frame of the first embodiment. In particular, the cross-sectional views of FIG. 1 correspond to a cross section taken along the line D1-D2 of FIG. 9(a). In FIG. 11, the reference numeral 1110 denotes a lead frame blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1160 second concave portions, 1170 flat surfaces, and 1180 an etch-resistant layer. First, a water-soluble casein resist using potassium dichromate as a sensitive agent is coated
5 over both surfaces of the lead frame blank 1110 made of a 42% nickel-iron alloy and having a thickness of about 0.15 mm. Using desired pattern plates, the resist films are patterned to form resist patterns 1120A and 1120B having first opening 1130 and second openings 1140, respectively
10 (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead frame blank 1110 to have a flat etched bottom surface to a thickness smaller than that of the lead frame blank 1110 in a subsequent process. The second openings 1140 are adapted
15 to form desired shapes of tips of inner leads. Although the first opening 1130 includes at least an area forming the tips of the inner leads 1110, a topology generated by partially thinned portion by etching in a subsequent process can cause hindrance in a taping process or a
20 clamping process for fixing the lead frame. Thus, an area to be etched needs to be large without being limited to fine portions of the tips of the inner leads. Thereafter, both surfaces of the lead frame blank 1110 formed with the resist patterns are etched using a 48 Be' ferric chloride
25 solution of a temperature of 57°C at a spray pressure of

2.5 kg/cm². The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth h corresponding to $1/3$ of the thickness of the lead frame blank 1110. FIG. 11(c).

5 Although both surfaces of the lead frame blank 1110 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in
10 this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the
15 resist pattern 1120B is formed. Subsequently, the surface provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Inctec Inc.) by a die coater to form an etch-resistant
20 layer 1180 so as to fill up the first recesses 1150 and to cover the resist pattern 1120A (FIG. 11(c)).

25 It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that the etch-resistant layer 1180 be coated over the entire

portion of the surface formed with the first recesses
and first opening 1130, as shown in FIG. 11(c), because
it is difficult to coat the etch-resistant layer 1180 on
the surface portion including the first recesses.
5 Although the etch-resistant layer 1180 wax employed in
this embodiment is an alkali-soluble wax, any suitable
wax resistant to the etching action of the etchant solution
remaining somewhat soft during etching may be used.
The method for forming the etch-resistant layer 1180 is not limited
10 to the above-mentioned wax, but may be a wax of a UV-se
type. Since each first recess 1130 etched by the pre-
etching process at the surface formed with the pattern
is adapted to form a desired shape of the inner lead frame
blank filled up with the etch-resistant layer 1180, it is
15 further etched in the following secondary etching process.
The etch-resistant layer 1180 also enhances the mechanical
strength of the lead frame blank for the second etching
process, thereby enabling the second etching process to be
conducted while keeping a high accuracy. It is
20 possible to enable a second etchant solution to be sprayed
at an increased spraying pressure, for example, 2.5 kg
or above, in the secondary etching process. The increased
spraying pressure promotes the progress of etching in the
direction of the thickness of the lead frame blank in the
25 secondary etching process. Then, the lead frame blank

portion of the surface formed with the first recesses
and first opening 1130, as shown in FIG. 11(c), being
is difficult to coat the etch-resistant layer 1180 on
the surface portion including the first recesses

5 Although the etch-resistant layer 1180 wax employed in
embodiment is an alkali-soluble wax, any suitable
resistant to the etching action of the etchant solution
remaining somewhat soft during etching may be used.

for forming the etch-resistant layer 1180 is not limited
10 the above-mentioned wax, but may be a wax of a UV-se
type. Since each first recess 1150 etched by the pre-
etching process at the surface formed with the paste
adapted to form a desired shape of the inner lead tip

filled up with the etch-resistant layer 1180, it is
15 further etched in the following secondary etching process.
The etch-resistant layer 1180 also enhances the mechanical
strength of the lead frame blank for the second etching
process, thereby enabling the second etching process to
conducted while keeping a high accuracy. It is

20 possible to enable a second etchant solution to be sprayed
at an increased spraying pressure, for example, 2.5 kg
or above, in the secondary etching process. The increased
spraying pressure promotes the progress of etching in
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surfaces 131Aa of the tips of the inner leads as shown in
FIG. 1, are flushed with one surfaces of remaining portions
of the inner leads having the same thickness with the lead
frame while being opposed to the second surfaces 131Ab, and
5 the third and fourth surfaces are formed to have a concave
shape which is depressed toward the inside of the inner
leads. Where a semiconductor chip is mounted on the second
surfaces 131Ab of the inner leads by means of bumps for an
electrical connection therebetween, as in a semiconductor
10 device according to a third embodiment as will be described
hereinafter, an increased tolerance for the connection by
bumps is obtained when the second surface 131Ab has a
concave shape depressed toward the inside of the inner
lead. To this end, an etching method shown in FIG. 12 is
15 adopted in this case. The etching method shown in FIG. 12
is the same as that of FIG. 11 in association with its
primary etching process. After completion of the primary
etching process, the etching method is conducted in a
manner different from that of the etching method of FIG. 11
20 in that the second etching process is conducted at the side
of the first recesses 1150 after filling up the second
recesses 1160 by the etch-resist layer 1180, thereby
completely perforating the second recesses 1160. At this
time, by implementing the primary etching process, etching
25 at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 131Ab, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGs. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGs. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness t of the inner lead tip which is finally obtained. For example, where the blank has a thickness t reduced to 50 μm , the inner leads can have a fineness corresponding to a lead width W_1 of 100 μm and a tip pitch p of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness t of about 30 μm and a lead

width W_1 of 70 μm , it is possible to form inner leads having a fineness corresponding to an inner lead pitch p of 0.12 mm. Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness t and the lead width W_1 . That is to say, an inner lead tip pitch p up to 0.08 mm, a blank thickness up to 25 μm , and a lead width W_1 up to 40 μm can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(1). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(1) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 (a polyimide tape is generally used, as shown in FIG. 9(c)(A)). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(D), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereon. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

10 The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(1)(a). The tip 131A has an etched flat surface (second surface) 131Ab which is substantially flat and therefore has a width W1 slightly greater than the width W2 of an opposite surface. The widths W1 and W2 (about 1000 μ m) are more than the width W at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(D)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(II)(a), there has particularly excellent in wire-bonding property, because the etched flat surface does not have roughness. FIG. 13(I) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared to that of the etched flat surface of this first embodiment. FIG. 13(II) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(II). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(II)(a) or FIG. 13(II)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will be described hereinafter. FIGs. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGs. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified

example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device, 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 270, and the semiconductor chip 210 is electrically connected at its electrodes (pads) 211 to the second surfaces 231a of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 211 is fastened together with the inner leads 231 by the reinforcing fastener tape 270. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230 as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(1), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(2), which performs a reinforcing function is used.

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGs. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG.

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of the this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of this third embodiment, the semiconductor chip 310 is fastened to the second surfaces 331Ab of the inner leads 331 by the bumps 311 thereby to be electrically connected to the second surfaces 331Ab. The lead frame 300 has a contour as shown in FIGs. 10(a) and 10(b), which is formed by the etching process of FIG. 11. As shown in FIG. 13(1)(b), both widths W1A and W2A (about 100 μ m) at top and bottom ends of the inner leads 331 are larger than a width WA at a center portion in a thickness-wise direction. Due to the fact that the second surfaces 331Ab of the inner leads 331 is depressed toward the inside of the inner leads and the first surfaces 331Aa are flat, a desired fineness can be obtained. Also, when the second surfaces 331Ab of the inner leads 331 are electrically connected to the semiconductor chip via bumps, easy connection can be accomplished as shown in FIG. 13(2)(b). Further, in the case of this third embodiment, as in the case of the first and second embodiments, the electrical connection between the resin-encapsulated semiconductor device 300 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 300 via the terminal portions 333A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 333A located on the top surfaces of the terminal

columns 333, respectively.

In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

portions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

5 Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line 10 B7-B8 of FIG. 7(b). Because an outer appearance of the semiconductor device of the this fourth embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing reference numeral 400 represents a semiconductor device, 15 410 a semiconductor chip, 411 pads, 430 a lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surface, 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating adhesive. In the semiconductor device of this fourth 20 embodiment, one surface of the semiconductor chip 410 on which the pads 411 are disposed is fastened to the second 25

surfaces 431Ab of the inner leads 431 by the insul
adhesive 470, and the pads 411 and the first surfaces
of the inner leads 431 are electrically connected with
other by wires 420. The semiconductor device of
5 fourth embodiment uses the same lead frame which is use
the third embodiment, which has the contour as shown
FIG. 10(a) and 10(b). Also, in the case of this fourth
embodiment, as in the case of the first and second
embodiments, the electrical connection between the res
10 encapsulated semiconductor device 400 of this embodiment
and an external circuit is achieved by mounting the res
encapsulated semiconductor device 400 via the terminal
portions 433A each being made of a semi-spherical solder
on a printed circuit substrate, with the terminal portion
15 433A located on the top surfaces of the terminal columns
433, respectively.

FIG. 7(d) is a cross-sectional view illustrating
modified example of the semiconductor device in accordance
with the fourth embodiment of the present invention. In
20 the modified example of the semiconductor device as shown
in FIG. 7(d), the terminal portions each comprising the
semi-spherical solder are not provided, and the top
surfaces of the terminal columns are directly used as the
terminal portions. Because the protective frame is not
25 used and the side surfaces 433B of the terminal columns 433

are exposed to the outside, a checking operation by a test, etc. can be easily performed.

(EFFECTS OF THE INVENTION)

3 The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having outer leads as shown in FIG. 13(b). As a result of this, the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem associated with coplanarity. In addition to these advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay time.

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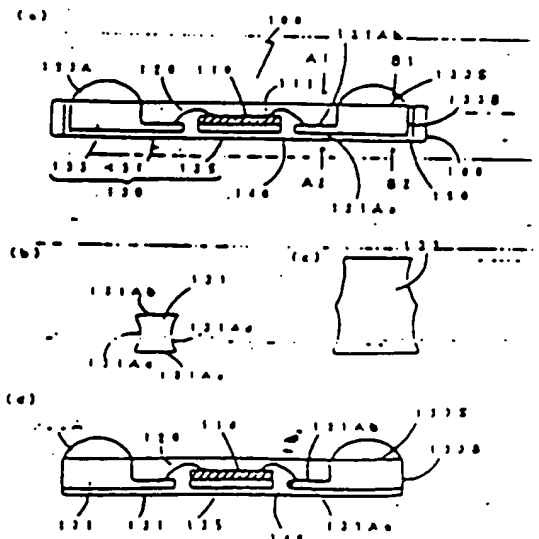
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(11) (五) (修正)

〔目的〕 多角化に対応して、且つ、アフターリードの迅速な平準化の両面に於いて、その業務の効率化を図る。……

(構成) 一般的に連結したリードフレーム形状と同じ部品の外装部品と接続するたりの比較の端子座133とを有し、且つ、端子座はインナーリードの外装側においてインナーリードに対して部材方向に突出して設けられており、端子座の先端部に半導体からなる端子部を設け、端子部を防止用部材から突出させて、端子座の外装側の側面を防止用部材から突出させて、インナーリードは、側面形状が略円形であり図131A、図2図A、図3図A、図4図Aの4図を有しており、かつ第1図はリードフレーム形状と同じ部品の他の部分の一方の面と同一平面上にあって第2図に面を合っており、第3図、第4図はインナーリードの内部に向かってんだん形状に変化させている。



(4) 株式の取得

【図55】 2面ニツチング加工によりインターリードの面をリードフレーム材の面より厚肉に形成せられたリードフレームを用いた装置に於て、前記リードフレームは、リードフレーム面より厚肉のインターリードと、該インターリードに一対的に連結したリードフレーム面と同じ厚さの外縁部とを形成するための仕状の導子柱とを有し、且つ、導子柱はインターリードの外縁部においてインターリードに対して所与方向に傾いて設けられており、導子柱の外縁面に半田がなる導子部を設け、導子部を禁止層部材から成らせ、導子柱の外縁部の傾斜を禁止層部材から成らせており、インターリードは、断面形状が矩形で第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム面と同じ厚さの他の部分の一方の面と同一平面上にあって第2面に向合っており、第3面、第4面はインターリードの内側に所かつて凹んだ形状に形成されていることを特徴とする座持禁止装置に於て。

(特許第2) 2 輪ニッティング機ニよりインターリードの部がリードフレーム基材の基より上面に外を加工されたリードフレームを用いた基を基であつて、前記リードフレームは、リードフレーム基材より上面のインターリードと、該インターリードに一時的に接合したリードフレーム基材と同じ部との外面面とを形成するための凸状の端子部とを有し、是つ、端子部はインターリードの外周面においてインターリードに対して傾く方向に直交して設けられており、端子部の突端の一部を防止用層層部から露出させて端子部とし、端子部の外面側の側面を防止用層層部から露出させており、インターリードは、前記基板が1層面であり、第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム基材と同じ部とその他の部分の一方の面と同一二面とに於て第2面に向を合せており、第3面、第4面はインターリードの内側に向つて凹んだ形状に形成されていることを特徴とする原形防止型ニッティング機。

(おまけ) 図式がないし？において、半導体原子はインターリード間にあり、金属原子の電極側はワイヤにてインターリードと金属側に接続されていることを知得とする回路設計が半導体電極。

【注5】 図表3において、リードフレームにダイパッドを有しており、半導体素子にダイパッド上に搭載され、固定されていることを特徴とする装置は、本発明である。

【図57】 は図56において、リードフレームはダイパッドを隔たないもので、半導体素子にインターリードととりに導電性金属テープにより固定されていることを特徴とする密封防止型半導体装置。

(図式例6) 図式例1ないし7において、本図式例は平成5年度分の当座預金の振替簿の表をインターリードの第2版

に絶縁性材料により固定されており、該絶縁性材料の
電線はワイヤによりインナーリードの溝に亘る位置
に固定されていることを保証とする突起状の型による
取。

(図 27) 図 26 がない 2 において、ホムロニ
はパンパによりインターリードの第 2 面に固定されて
同時にインターリードと連動していることが知られて
いる。

(月 日 年 月 日)

(0 0 0 1)

(屋上との共用部分) 玄関には、車庫は床の高さにより
に対応して、主として、アフターリートの高さは（スニ
ー）やアフターリートの高さ（コブラデリアー）の
高さに合わせて、リードフレームを用いた構造に
車庫を設ける。

(0 0 0 2)

(反張の区域) 反張より用いられている原理防止型の半導体装置(プラズマチックリードフレームパッケージ)は、一般に図15(1a)に示されるような構造であり、半導体素子1510を保護するダイパッド5111・110の両側の区域との電気的接続を行うためのアウターリード1511・13、アウターリード5110に一体となったインナーリード1511・12、インナーリード5111・12の先端部と半導体素子1520との電極パッド1521とを電気的に接続するためのワイヤ1530、半導体素子1520を固定して基板からの応力、圧縮から守る樹脂1540部からなっており、半導体素子1520をリードフレームのダイパッド1511・110部に固定した方法には、樹脂1540により防止してパッケージとしたもので、半導体素子1520の電極パッド1521に対応できる数のインナーリード1511・12を必要とするものである。そして、このような原理防止型の半導体装置の見立図として用いられる(参照)リードフレームは、一般に図15(1b)に示すような構造のもので、半導体素子を保護するためのダイパッド1511と、ダイパッド1511の両端にはけられた半導体素子と接続するためのインナーリード1511・12、インナーリード1511・12に連続して形成部との電気を行うためのアウターリード1511・13、原理防止する鋼のダムとなるダムバー1514、リードフレーム1510全体を支持するフレーム(基)51515を備えており、通常、コパール、42合金(42Xニッケル-合金)、銅合金のような金属に形成した金属をいい、プレス加工したエッチングによって形成されている。但、図15(1b)(c)は、図15(1b)(1)に示すリードフレーム51515のF1-F2にみける半導体装置である。

て、テーピングの工程や、リードフレームを固定するクランプ工程で、ベタ状に固定された部分に生じた歪みなどの影響が原因になる場合があるので、エッチングを行うエリアはインターリード部分の周辺加工部分だけにせず、せめてところどころがある。ないで、温度 57°C、比重 4.8 ポーラの酸化第二銅溶液を用いて、スプレーした、5 kg/cm² にて、レジストパターンが形成されたリードフレームを 40 分 110°C の温度でエッチングし、ベタ（平基板）に固定された第 2 の部材 1150 の固定部がリードフレーム部材の約 2/3 程度に達した時点でエッチングを止めた。（図 11（b））

上又は1回目のエッチングにおいては、リードフレーム
は1110の位置から同時にエッチングを行ったが、
必ずしも位置から同時にエッチングするを要しない、本
実施例のように、第1回目のエッチングにおいてリード
フレームは1110の位置から同時にエッチングする
理由は、位置からエッチングすることにより、後述す
第2回目のエッチング時に使用するため、レジスト
パターン9208面からのみの片面エッチングの場合と
比べ、第1回目エッチングと第2回目エッチングのトー
タル時間が短縮される、次いで、第一の面に1100
面の位置された第一の凹部1500内にエッチング抵抗
1180としての銅エッチング面の有るポットメルト型
フッ素スプレーインクエッチング抵抗のフッ素系樹脂
(MR-WB6)を、ダイコータを用いて、塗布し、ペ
タ板(平電板)に露せられた第一の凹部1500に埋め込
んだ、レジストパターン1120A上およびエッチング抵
抗層1180に露せられた板面とした、(図11)

エッチングを減らし、レジストパターンは、
— 0.4と全正に一致する必要があるが、別の部分、1.5
0を減じ一減にのみ一致することは望みに、図11

(c) に示すように、第一の凹部 1:50 とともに、第一の凹部 1:130 が完全にエッチング抵抗層 1:80 を形成した。本実施例で使用したニッチング抵抗層 1:80 は、アルカリ性塩のワックであるが、基本的にエッチング時に耐性があり、ニッチング時にある程度の膨張のあめしものがあり、特に、上記ワック系に固定されて、UV 硬化型のものではないことによりニッチング抵抗層 1:80 をインワード先端部の膨張を防止するためのパターンが形成された後部の凹部と第一の凹部 1:50 につづかなことにより、後者のニッチング時に第一の凹部 1:50 が膨張されて穴とならないようにしていることとし、両端部はニッチング加工に対しての機械的な強度確保をしており、スプレッドを (2.5 kg/cm² 以上) とすることから、これによりニッチングが仮に方向に進行しなくなると、この後、第二凹部のニッチングを所望（本実施例）に形成された第二の凹部 1:60 を正面からリードフレームと重なり 1:10 をエッチングし、直進させ、

インターリードエラーは131人を経験した。(5: ;
(c))

第1回目のエッチング加工にて作製された、リードフレーム面に形成したエッチング抵抗面に矛盾であるが、この面を第2面にインターリード部にへこんだ面である。従って、従来、エッチング抵抗層9200のレジスト膜(レジストパターン1120A、1120B)の形成を行い、インターリード部は2131Aが2層に成膜された図9に示すリードフレーム120Aを形成した。エッチング抵抗層1120とレジスト膜(レジストパターン1120A、1120B)の形成に必要としたトリウム塩溶液により腐食が生じた。

(0014) 上記、図1に示すリードフレームの加工方法に、本発明に用いられる、インターリード先を自動的に形成したリードフレームをエッチング加工により露通する手段で、特に、図1に示す、インターリード先部の第1面131Aを露通形成した後の状態と同一面に、第2面131Bと対向させて形成し、また、図1面131A、第2面131Bをインターリードの内側に向かって凹んだ花形にするエッチング加工方法である。前述する本発明の第2面形成のようにパンプを用いて第2面形成をインターリードの第2面131Bに形成し、インターリードと電気的に接続する場合に

二、第二図1、3、1Aもインターリード側に付いた発生に
対応した方がパルス発生の際の許容度が大きくなる
。図12に示すニッチング加工方法が知られる。図1
2に示すエッチング加工方法に、第1回目のエッチン
グ工程では、図11に示す方法と異じてあるが、エッチ
ング後、図1180も第二の図1160側に延びた
。第一の図1150側から第二図8のニッチング
を行い、第二図8まで延びておる。図1180、第一
のニッチングにて、第二図8より1400側のニッチ
ングを充分に行つて、図12に示すニッチング加工
法によつて得られたリードフレームのインターリード
発生部は、図16(b)に示すように、第二図3
1Aもインターリード側に付いた図16(a)になる。

(0015) 図、と図11、図12に示すエッチング加工方法のように、エッチングを2段階にわたって行うエッチング加工方法を、一般には2段エッチング加工方法とされており、上述工程に有利な加工方法である。本発明に於いて図9(a)に示す、リードフレーム130Aの加工においては、2段階のエッチング加工で、パッド形成を工程することにより部分的にリードフレームを薄くしながら外周加工をする方法とが採用して行われており、リードフレームを薄くした部分において、図11、図12に示す、上述の方法においては、インターリード間距離131Aの形成加工は、その距離1360の基準と、最終的にはほぼインターリード間距離の長さ1に近等となるもので、例えば、距離1を50μm

の両面には平等ではあるが、この部分の両面が、
大きくとれない。また両面とリットフリーとは
である。結局「ボンディング」面には両面が、
ボンディング面より劣る。図13(2)に示す「ボン
ディング」によりインナーリット先頭部を固定した後に
ボンディング面によりインナーリット先頭部(133)に
1331Dを加えたものの、両面両面(図13)で
この面(ボンディング)を示したものであるが、こ
れは両面が図に示すように両面になっている
ため、どちらの面を用いても「ボンディング」して
b. 図13(2)の(a)、(b)に示すように両面
(ボンディング)の面に両面が速く品質的に劣る
場合が多い。図1331Aは両面ボンディング面

(0018) 次に実施例1の駆動防止型ニギハヤヒ型のス
クローを挙げる。図3(a)～図3(e)に、それぞれ、
は実施例1の駆動防止型ニギハヤヒ型のスクローの断面図
である。図3(a)に示すスクローのニギハヤヒ部は、実施例
1のニギハヤヒ部とは、ダイバッド135の位置が異なる
もので、ダイバッド部135が外周面に突出している。ダイ
バッド部135が外周面に突出していることにより、ス
クロー1に比べ、他のスクローが傾いてゐる。図3(b)に
示すスクローのニギハヤヒ部は、ダイバッド部135が外周
面に突出させているものであり、実施例1に比べ、他のス
クローが傾いている。実施例1や図3(a)に示すスクロー
とは、ニギハヤヒ部110の中心が異なり、ワイヤポンチ
ング部をリードフレームの裏面に設けている。図3
(c)～図3(d)～図3(e)に示すスクローは、それ
ぞれ実施例1、図3(a)に示すスクロー、図3(b)に
示すスクローにおいて、ニギハヤヒ部からなるニギハヤヒ部を設
けず、送り部の面を駆動部と駆動部とを用いているもので
あり、製造工程を単純化した構造となつてゐる。

[illegible]

リードフレームの図

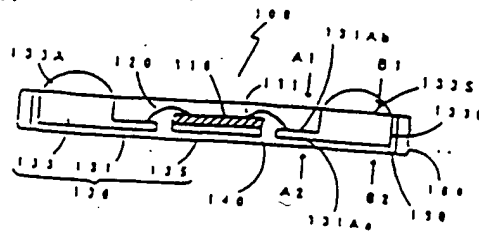
0

190
 260
 270
 350
 470
 1110
 1120A, 1120B
 1130
 1140
 1150
 1160
 1170
 1180
 1320B, 1320C, 1320D
 1321B, 1321C, 1321D
 1331B, 1331C, 1331D
 1331A2

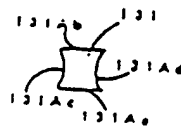
1331A2
 1410
 1420
 1430
 1440
 1510
 1511
 1512
 1512A
 1513
 1514
 1515
 1520
 1521
 1530
 1540
 止用器具

(21)

(a)



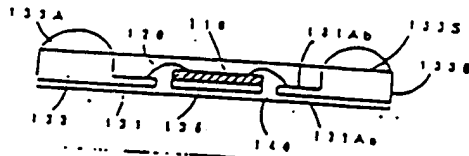
(b)



(c)

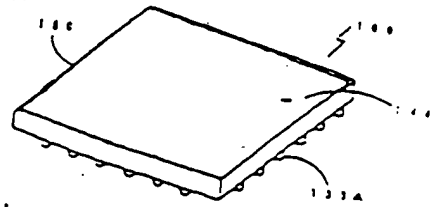


(d)



(22)

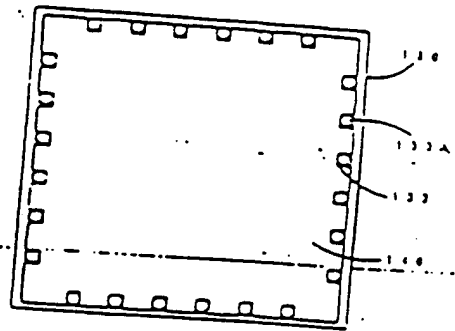
(a)



(b)

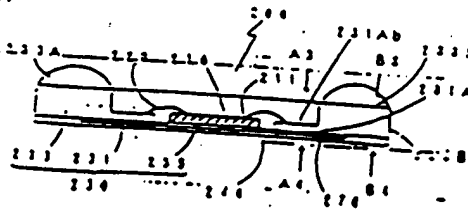


(c)

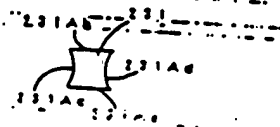


(24)

(a)



(b)

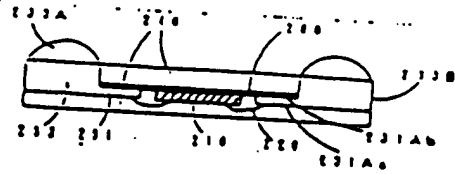


(c)

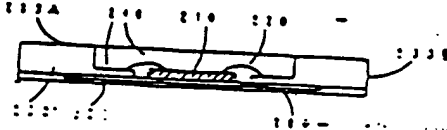


(25)

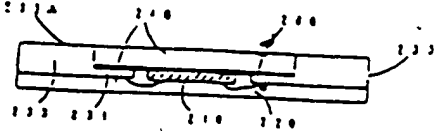
(a)



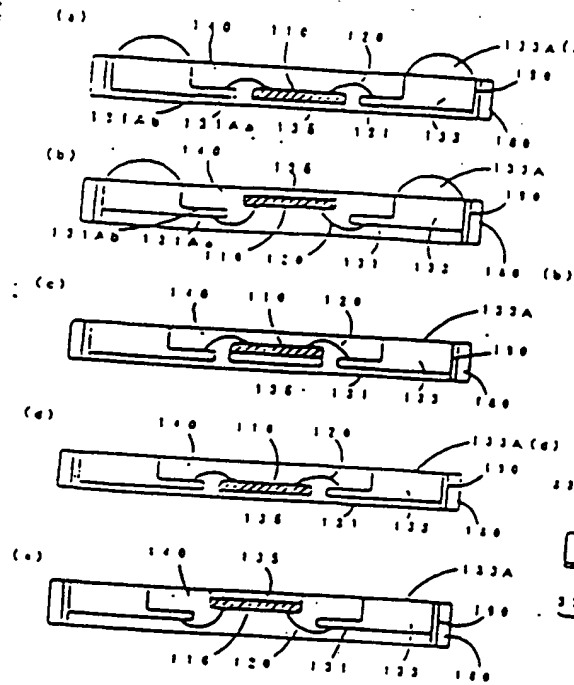
(b)



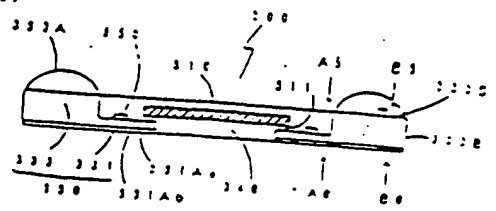
(c)



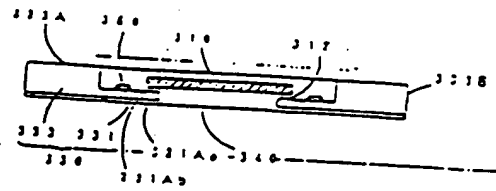
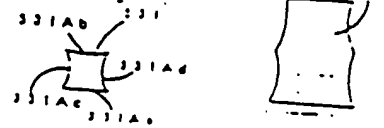
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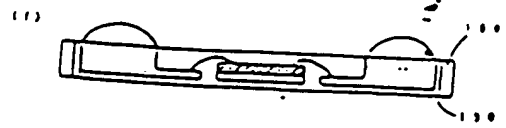
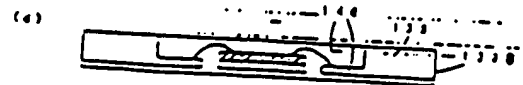
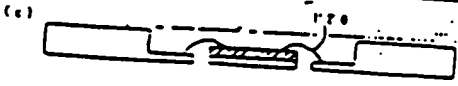
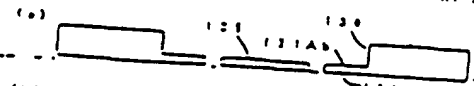
(26)



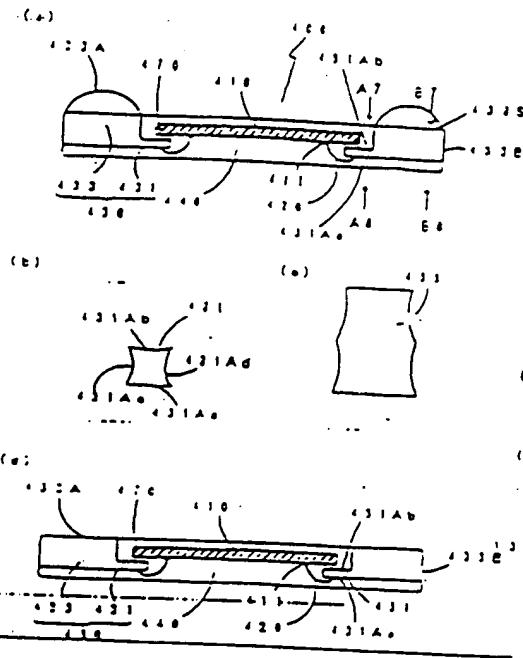
(c)



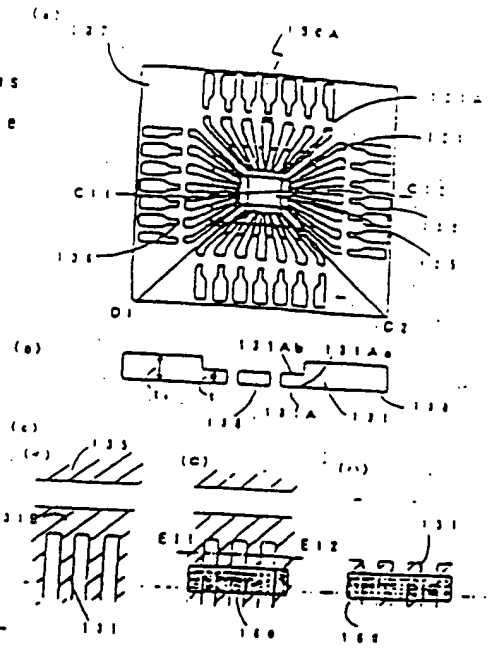
(23)



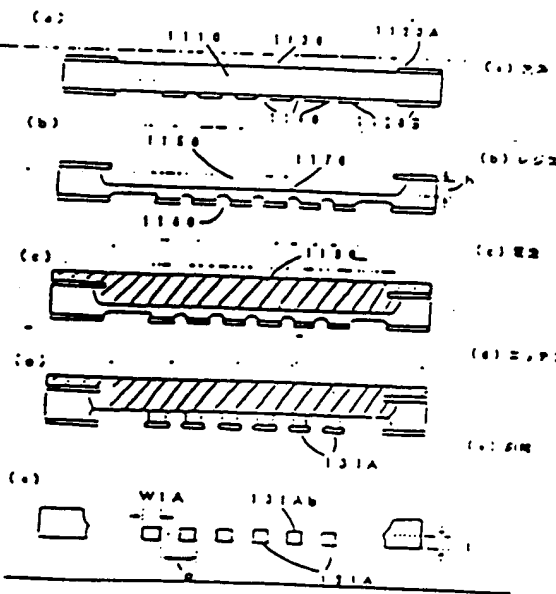
(27)



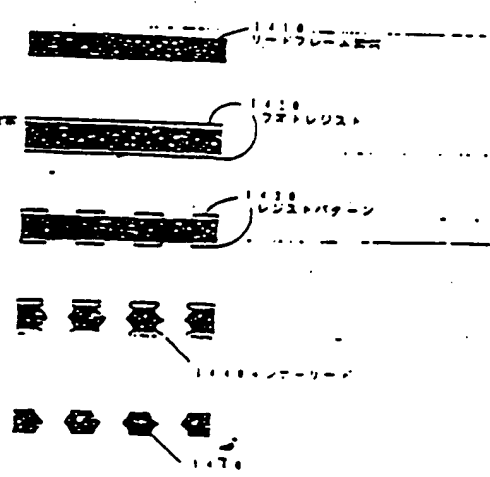
(29)



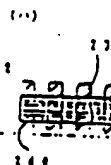
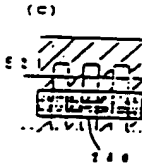
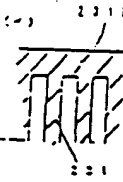
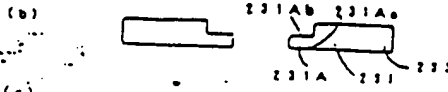
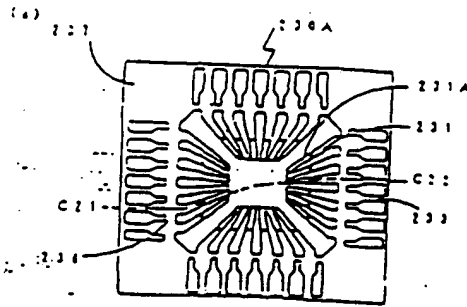
(31)



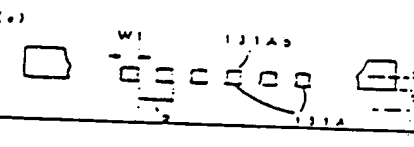
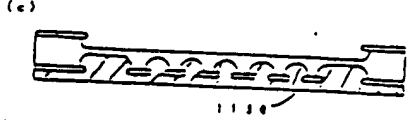
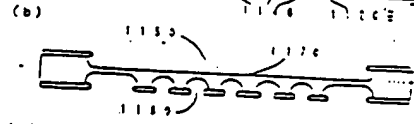
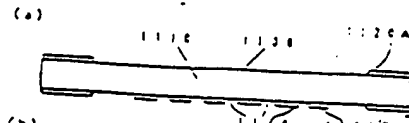
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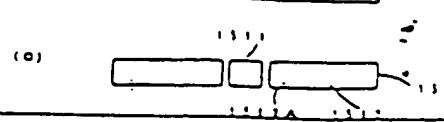
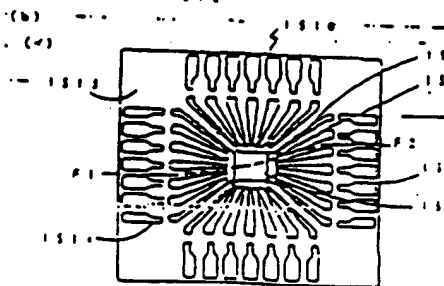
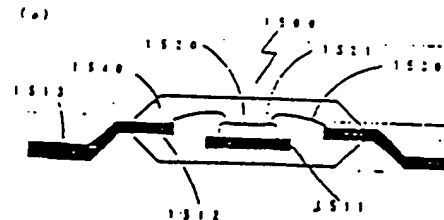
(210)



(212)



(215)



(213)

